

FIG.1A
PRIOR ART

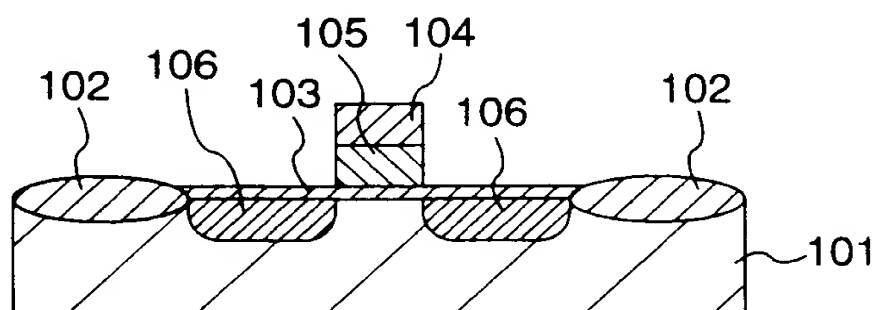


FIG.1B
PRIOR ART

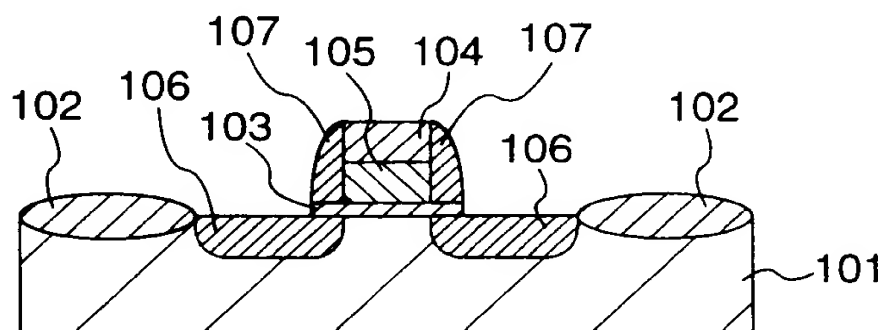


FIG.1C
PRIOR ART

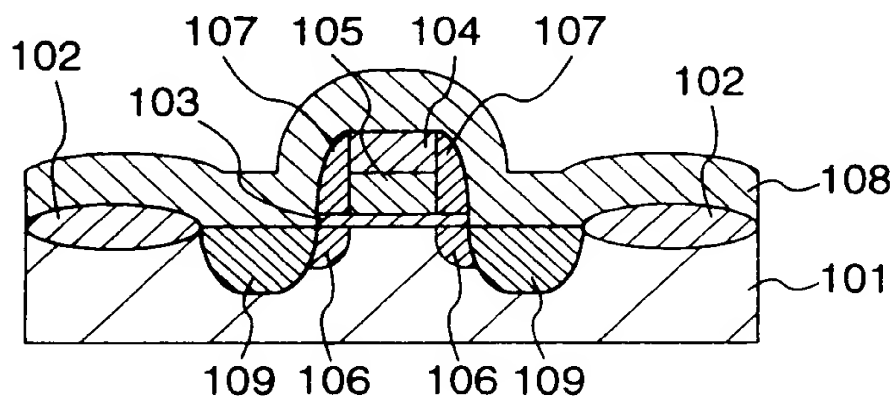


FIG.1D
PRIOR ART

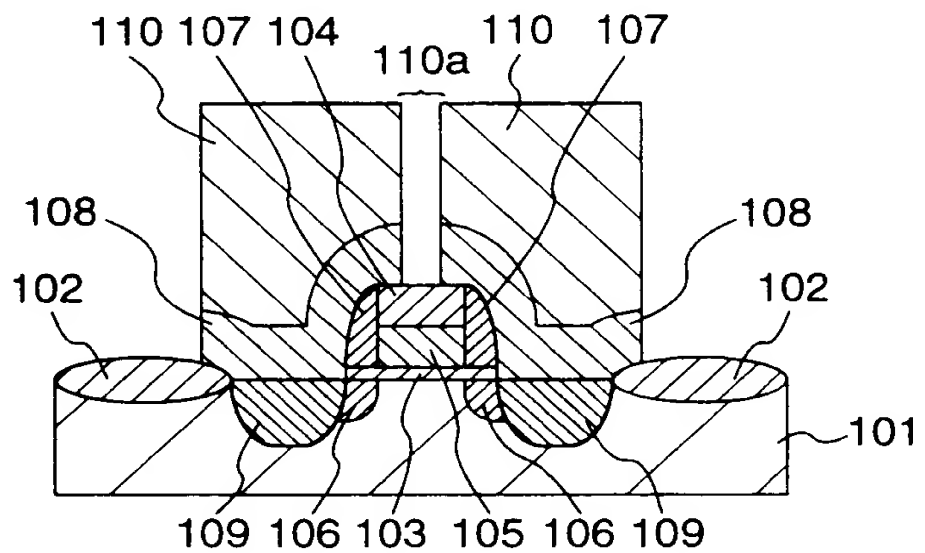


FIG.1E
PRIOR ART

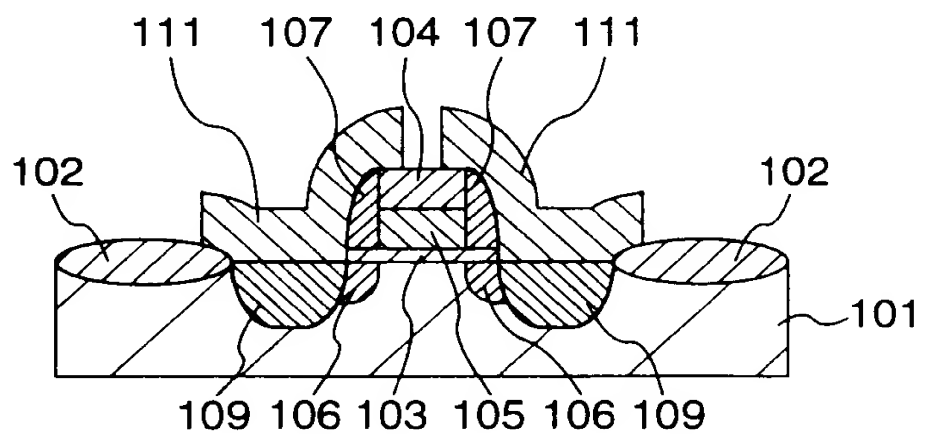


FIG.2
PRIOR ART

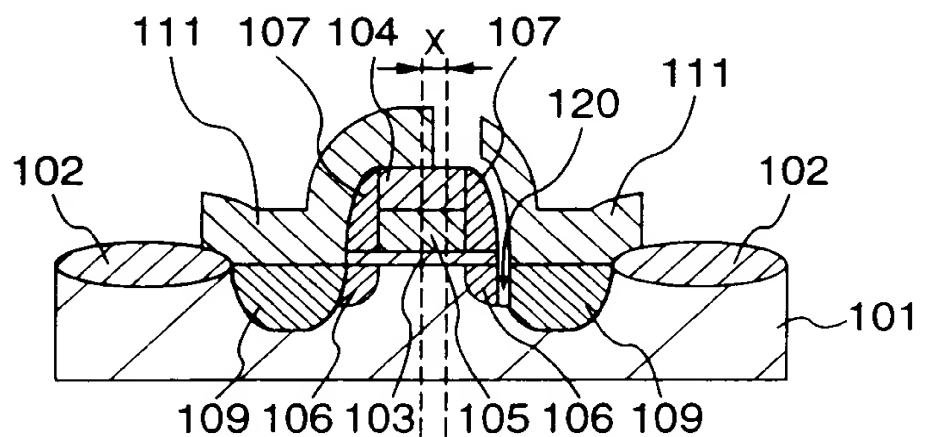


FIG.3A

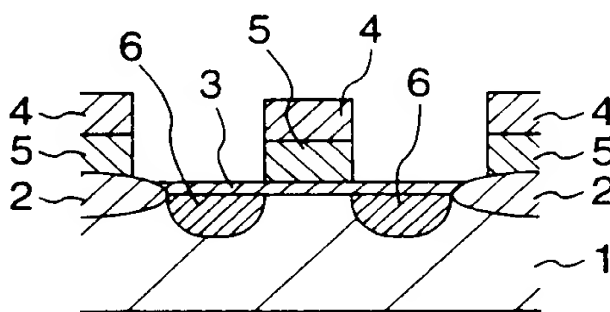


FIG.3B

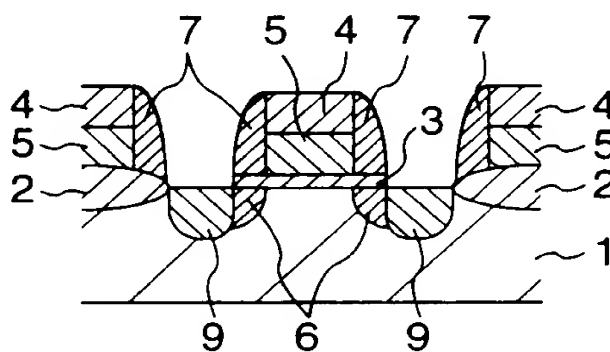


FIG.3C

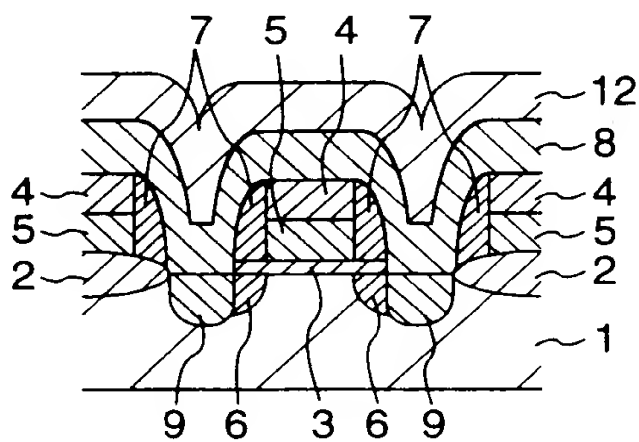


FIG.3D

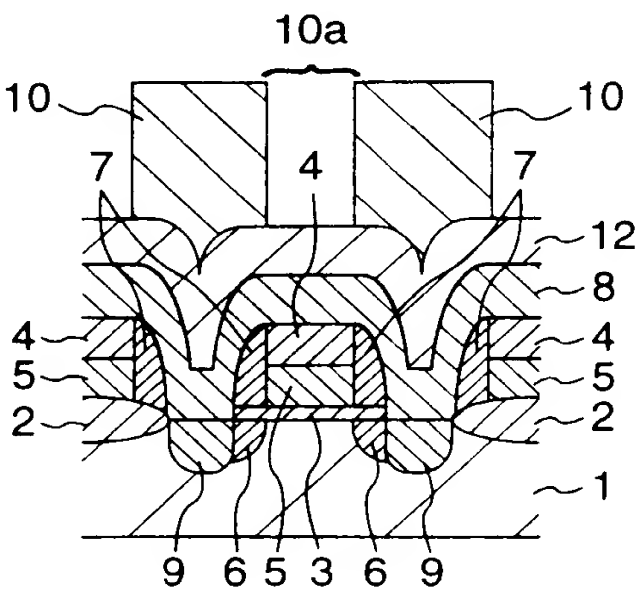


FIG.3E

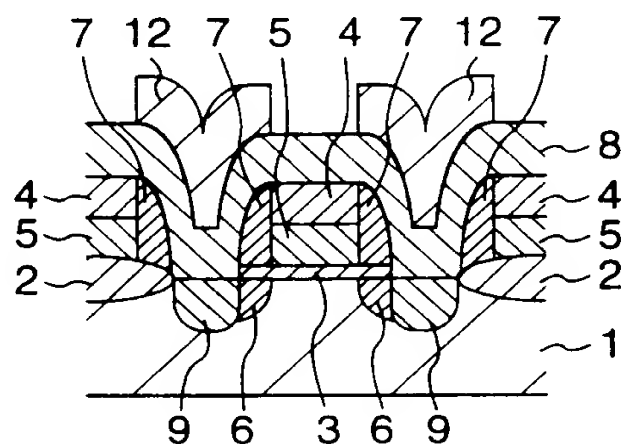


FIG.3F

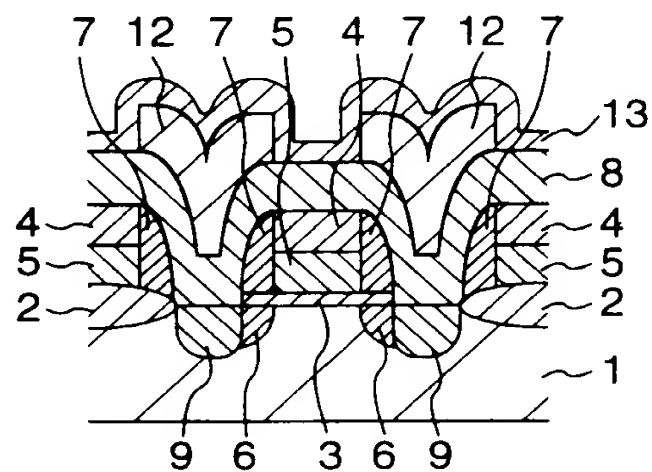


FIG.3G

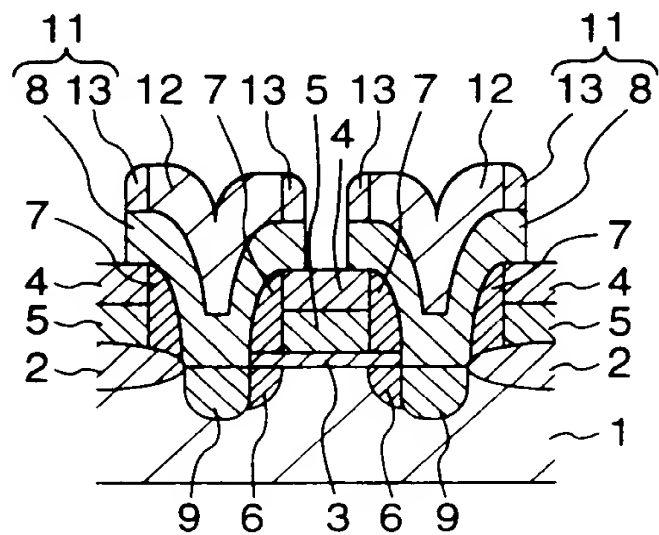


FIG.3H

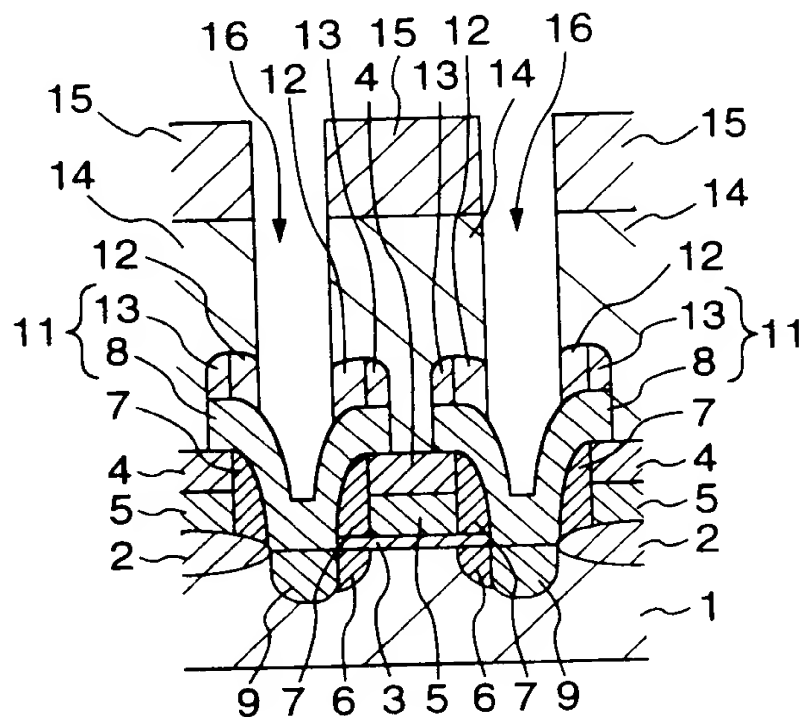


FIG.3I

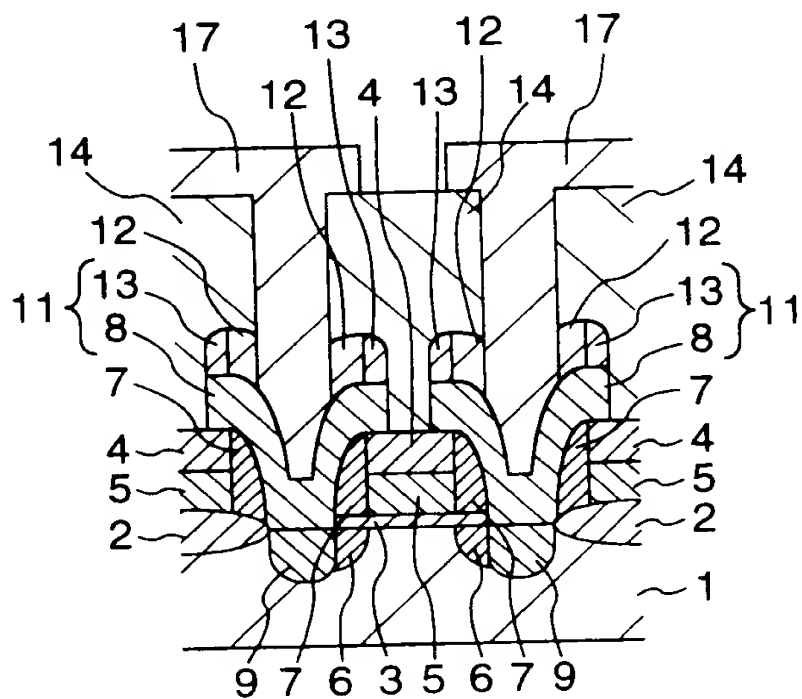


FIG.4

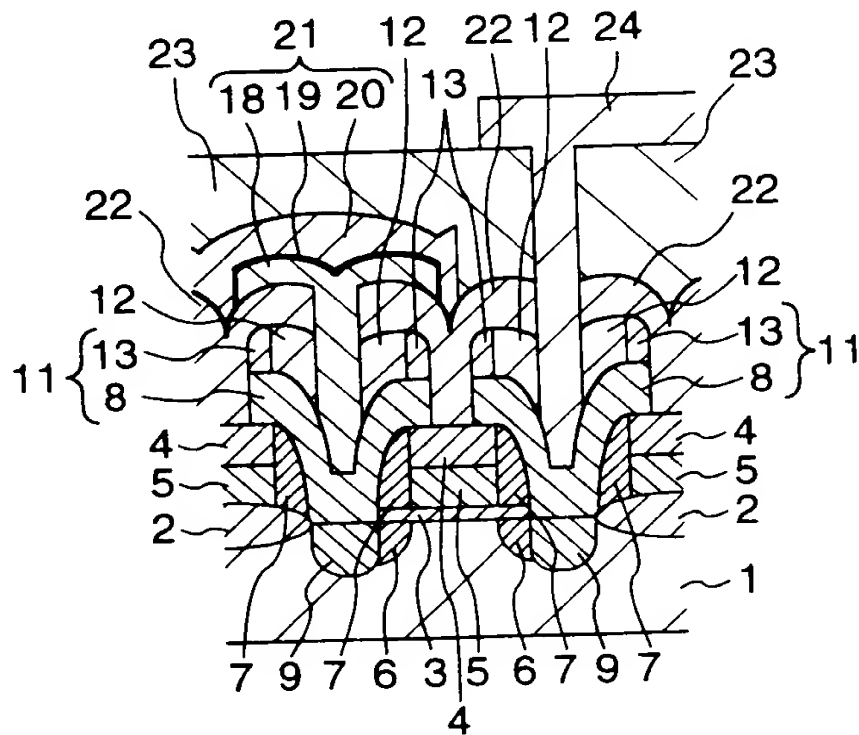


FIG.5

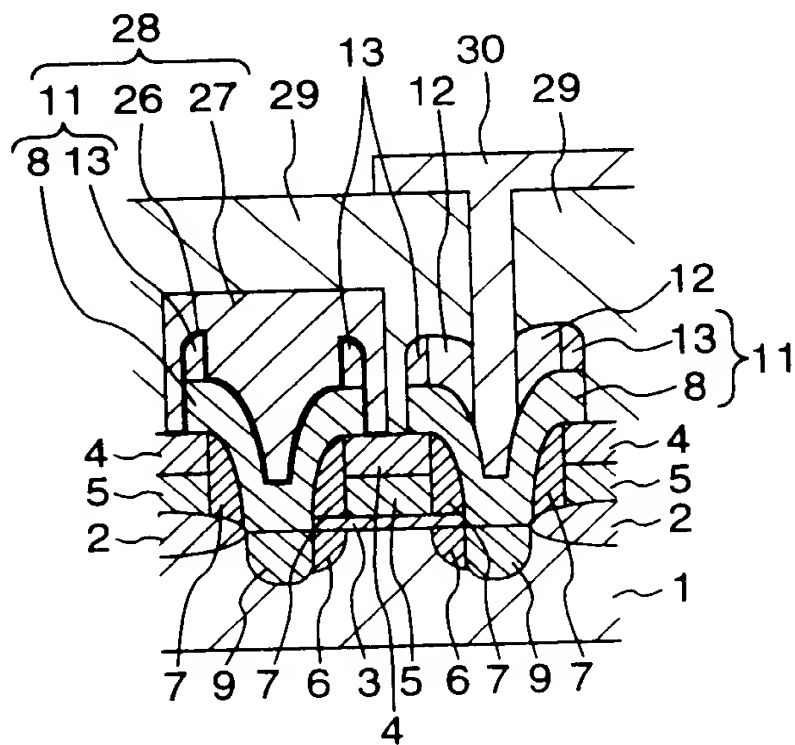


FIG. 6A

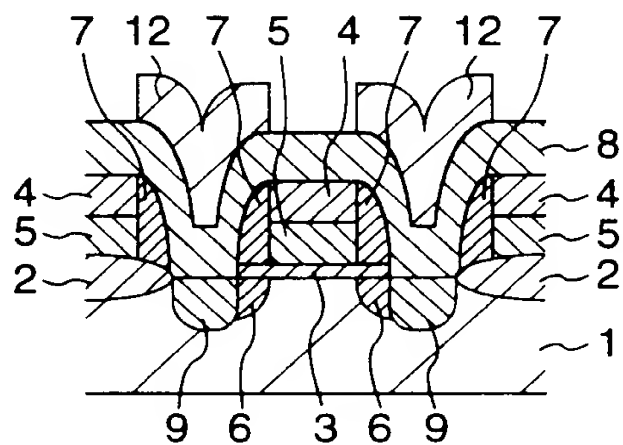


FIG. 6B

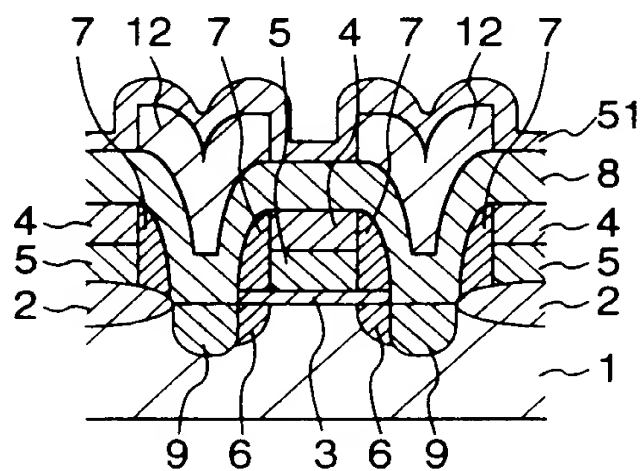
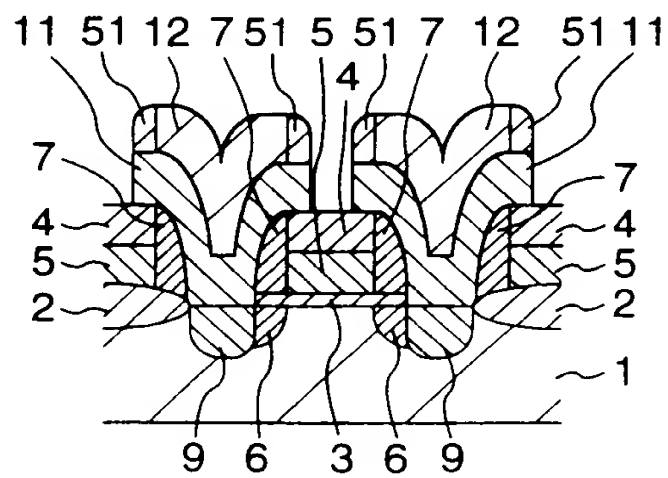


FIG. 6C



The diagram shows a cross-section of a semiconductor device. At the bottom is a substrate 1. Above it is a base layer 2. On the base layer, there are three main regions: 4, 5, and 7. Regions 4 and 5 each have a central vertical structure 11 surrounded by a material 12. Region 7 has a central vertical structure 14. The top surface of the device is labeled 15. Arrows point downwards from the top surface into the vertical structures, indicating incident light or signals.